CLAIMS

1. A method for forming on a substrate an electronic device including at least one electrically conductive material and one semiconductive material, the materials being deposited onto the substrate from respective liquids, the method comprising:

forming on the substrate a surface energy pattern that defines a first area of the substrate, a second area of the substrate spaced apart from the first area of the substrate by a spacing area, and a third area of the substrate at least partly overlapping the first area, the second area and the spacing area; and subsequently:

depositing the electrically conductive material on the substrate by applying the liquid comprising the electrically conductive material over the substrate; and

depositing the semiconductive material on the substrate by applying the liquid comprising the semiconductive material over the substrate;

wherein

the surface energy pattern is such as to localise the electrically conductive material to the first and second areas and to localise the semiconductive material to the third area; and

the semiconductive material is deposited so as to extend over the third area continuously between the conductive material in the first area and the conductive material in the second area.

2. A method as claimed in claim 1 wherein the semiconductive material is deposited so as to cover substantially the whole of the spacing area between the first area and the second area.

3. A method as claimed in claim 1 or claim 2 wherein the surface energy pattern is such that the semiconducting material is attracted more strongly to the spacing area than to the first and second areas.

4. A method as claimed in claim 1 or claim 2 wherein the surface energy pattern is such that the semiconductive material is attracted more strongly to the first and second areas than to the spacing area.

5. A method as claimed in any preceding claim wherein the surface energy pattern further comprises a fourth area surrounding the region comprising the first and second areas and the spacing area.

6. A method as claimed in claim 5 wherein the surface energy pattern further comprises a fifth area surrounding the fourth area.

7. A method as claimed in any preceding claim wherein the spacing area has a higher repellence for the conductive material than the first and second areas.

8. A method as claimed in claim 5 wherein the fourth area has a higher repellence for the semiconductive material than the third area.

9. A method as claimed in claim 2 wherein:

the surface energy pattern comprises further areas, one of the further areas being adjacent to a first end of the spacing area and another of the further areas being adjacent to an opposite end of the spacing area; and

the repellence of the further areas relative to the repellence of the spacing area to the liquid of the semiconductive material is such that on deposition of the semiconductive material the semiconductive material is encouraged to cover substantially the whole of the spacing area.

10. A method as claimed in any preceding claim, wherein the width of the spacing area between the first and second areas is less than 20 microns.

11. A method as claimed in any preceding claim, wherein the width of the spacing area between the first and second areas is less than 1 micron.

12. A method as claimed in any preceding claim, wherein the electrically conductive material formed in the first and second areas forms source and drain electrodes of a transistor.

13. A method as claimed in any preceding claim, wherein the semiconductive material formed in the third area is an active semiconducting island of a transistor.

14. A method as claimed in any preceding claim, wherein the surface energy pattern of the substrate is formed using fluorinated species.

15. A method as claimed in claim 14 wherein the surface energy pattern of the substrate is formed by exposure of the substrate to a plasma treatment.

16. A method as claimed in claim 15 wherein the surface energy pattern of the substrate is formed by exposure of the substrate to a CF_4 plasma treatment.

17. A method as claimed in claim 14 wherein the surface energy pattern of the substrate is formed by exposure of the substrate to a fluorinated self-assembling monolayer molecule.

18. A method as claimed in any preceding claim, wherein the surfaces of the first and second areas are of substantially identical composition.

19. A method as claimed in any preceding claim, wherein the first and second areas are formed on an exposed surface of a layer deposited on a planar structural member.

20. A method as claimed in any preceding claim, wherein the surface of the substrate has a lower surface roughness in the first and second areas than in regions surrounding the first and second areas.

21. A method as claimed in any preceding claim, wherein the viscosity of the liquid comprising the semiconductive material is higher than 5 cpi.

22. A method as claimed in any preceding claim, wherein the boiling point of the liquid comprising the semiconductive material is less than 180 °C.

23. A method as claimed in any preceding claim, wherein the substrate is held at a temperature above 40°C while the liquid comprising the semiconductive material is deposited.

24. A method as claimed in any preceding claim, wherein the temperature of the liquid comprising the semiconductive material is less than 20°C.

25. A method as claimed in any preceding claim, wherein a flow of gas is directed onto the substrate surface during the deposition of the semiconductive material.

26. A method as claimed in any preceding claim, wherein the contact angle difference of the liquid comprising the semiconductive material on the surface of the spacing area, is larger by more than 10° than its contact angle on the surface of the first and second areas.

27. A method as claimed in claim 26, wherein the contact angle of the liquid comprising the semiconductive material on the surface of the spacing area, is larger by more than 30° than its contact angle on the surface of the conductive material in the first and second areas.

28. A method as claimed in any preceding claim, wherein the contact angle of the liquid comprising the semiconductive material on the surface of the spacing area is smaller than 100°.

29. A method as claimed in claim 28, wherein the contact angle of the liquid comprising the semiconductive material on the surface of the spacing area is smaller than 60°.

30. A method as claimed in claim 19 wherein the thickness of said layer is less than 500 Å.

31. A method as claimed in claim 30 wherein the thickness of said layer is less than 200 Å.

32. A method as claimed in any preceding claim wherein the surface tension of said liquid comprising the semiconductive material is higher than 25 mJ / m^2.

33. A method as claimed in any preceding claim, wherein said electrically conductive or semiconductive material is deposited by droplet deposition.

34. A method as claimed in any preceding claim, wherein said electrically conductive or semiconductive material is deposited by ink-jet printing.

35. A method as claimed in any preceding claim wherein said electrically conductive material is a polymer.

36. A method as claimed in any of claims 1 to 34, wherein the electrically conductive material is an inorganic particulate material capable of suspension in the said liquid.

37. A method as claimed in any preceding claim, wherein the semiconductive material is a conjugated organic molecule.

38. A method as claimed in claim 37, wherein the semiconductive material is a conjugated polymer.

39. A method as claimed in any preceding claim as dependent on claim 6, wherein the spacing area, and the fourth area are less repulsive to the liquid comprising the semiconductive material than the first, second and fifth areas.

40. A method as claimed in claim 39, wherein the liquid comprising the conductive material is confined to the first and second area by the repellence of the fourth area and the spacing area, and the semiconductive material is confined to the third area by the repellence of the fifth area.

41. A method as claimed in claim 39 or 40, wherein the spacing area and the fourth area are of substantially identical surface energy.

42. A method as claimed in any of claims 39 to 41, wherein the first, second and fifth area are of substantially identical surface energy.

43. A method as claimed in any of claims 39 to 42, wherein conductive material is absent from the fifth area.

44. A method as claimed in any preceding claim wherein the liquid comprising the semiconductive material is capable of swelling the spacing area.

45. A method as claimed in claim 44, wherein the surface of the spacing area comprises a polymer that is swelled by the liquid comprising the semiconductive material on deposition of the semiconductive material.

46. A method as claimed in claim 45, wherein said polymer is a polymer containing an Si-O-Si moiety.

47. A method as claimed in claim 46, wherein the polymer is a polymer derived from a substituted benzocyclobutene.

48. A method as claimed in any preceding claim further comprising the step of depositing at least one further material on top of the conductive or semiconductive material.

49. A method as claimed in claim 48 wherein the further material is a dielectric material which is confined, on deposition, by the surface energy pattern.

50. A logic circuit, display, sensor or memory device formed by the method of any preceding claim.

51. A logic circuit, display, sensor or memory device comprising a plurality of transistors formed by the method of any of claims 1 to 49.